Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) An integrated circuit chip ~~with multiple wirebonds,~~ comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a second contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and ~~exposes~~ said first contact point is at a bottom of said first opening, ~~pad,~~ and wherein a second opening in said passivation layer is over a second contact point of said second contact pad, and ~~exposes~~ said second contact point is at a bottom of said second opening; ~~pad;~~

a power metal structure over said passivation layer and on said first contact point, ~~pad,~~ wherein said power metal structure is connected to said first contact point ~~pad~~ through said first opening, wherein said power metal structure comprises a copper layer, and wherein ~~one of said multiple wirebonds is bonded on~~ said power metal structure has a

first region used to be wirebonded thereto for connection made to a next level of packaging;

a ground metal structure over said passivation layer and on said second contact point, ~~pad,~~ wherein said ground metal structure is connected to said second contact point ~~pad~~ through said second opening, wherein said ground metal structure comprises a copper layer, and wherein ~~another one of said multiple wirebonds is bonded on~~ said ground metal structure has a second region used to be wirebonded thereto for connection made to said next level of packaging;

a capacitor over said passivation layer and directly over said first contact point; ~~pad exposed by said first opening;~~

a first solder contact ~~connection~~ directly over said first contact point and between said capacitor and said power metal structure, wherein said first solder contact connects ~~connecting~~ said capacitor to said power metal structure; and

a second solder contact ~~connection~~ between said capacitor and said ground metal structure, wherein said second solder contact connects ~~connecting~~ said capacitor to said ground metal structure.

Claims 2-3 (canceled)

4. (withdrawn -- currently amended) The integrated circuit chip according to claim 1 further comprising a polymer layer on ~~over~~ said passivation layer, wherein said power and ground metal structures are further on said polymer layer.

Claims 5-6 (canceled)

7. (previously presented) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a gold layer over said copper layer of said ground metal structure.

Claim 8 (canceled)

9. (currently amended) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and ~~exposes~~ said first contact point is at a bottom of said first opening, ~~pad,~~ and wherein said passivation layer comprises a nitride;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point ~~pad~~ through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact point, ~~pad,~~ and wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and over said second contact pad;

a solder contact ~~connection~~ between said capacitor and said second contact pad, wherein said solder contact ~~connection~~ connects said capacitor to said second contact pad; and

~~an additional metal layer~~ electroplated copper between said solder contact ~~connection~~ and said second contact pad.

10. (currently amended) The integrated circuit chip according to claim 9 further comprising a third contact pad over said semiconductor substrate, wherein said third contact pad has a second contact point under ~~exposed by~~ a second opening in said passivation layer, and said second contact point is at a bottom of said second opening, wherein said second contact point is used to be wirebonded thereto for connection made to a next level of packaging. ~~a wirebond on said third contact pad.~~

11. (currently amended) The integrated circuit chip according to claim 9 further comprising a third contact pad over said passivation layer, wherein said third contact pad is used to be wirebonded thereto for connection made to a next level of packaging. ~~and a wirebond on said third contact pad.~~

12. (currently amended) The integrated circuit chip according to claim 9 further comprising a third contact pad over said semiconductor substrate, wherein said third contact pad has a second contact point under ~~exposed by~~ a second opening in said passivation layer, and said second contact point is at a bottom of said second opening, and a fourth contact pad

on said ~~third~~ second contact point, ~~pad,~~ wherein said fourth contact pad is used to be wirebonded thereto for connection made to a next level of packaging. ~~and a wirebond on said fourth contact pad.~~

Claims 13-14 (canceled)

15. (currently amended) An integrated circuit chip ~~with a wirebond,~~ comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, and wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and ~~exposes~~ said first contact point is at a bottom of said first opening; ~~pad;~~

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point ~~pad~~ through said first opening;

a third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point ~~pad~~ through said first opening and connected to said second contact pad, wherein the position of said third contact pad from a top perspective view is different from that of said first contact point, ~~pad,~~ and wherein ~~said wirebond is bonded on~~ said third contact pad has a region used to be wirebonded thereto for connection made to a next level of packaging;

a first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and ~~exposes~~ said second contact point is at a bottom of said second opening; ~~pad;~~

a capacitor over said first polymer layer and over said second contact point; ~~pad;~~ and

a solder contact ~~connection~~ between said second contact ~~pad~~ point and said capacitor, wherein said solder contact ~~connection~~ connects said capacitor to said second contact point. ~~pad.~~

Claim 16 (canceled)

17. (previously presented) The integrated circuit chip according to claim 15, wherein said second contact pad comprises a gold layer.

18. (previously presented) The integrated circuit chip according to claim 15, wherein said second contact pad comprises a copper layer.

19. (currently amended) The integrated circuit chip according to claim 15, wherein a ground voltage is applied to ~~further comprising a ground metal structure connected to said capacitor, to said wirebond and to~~ said first contact pad.

Claim 20 (canceled)

21. (currently amended) The integrated circuit chip according to claim 15, wherein a power supply voltage is applied ~~further comprising a power metal structure connected to said capacitor, to said wirebond and~~ to said first contact pad.

22. (currently amended) The integrated circuit chip according to claim 15, wherein said second contact point ~~pad~~ is directly over said passivation layer.

Claims 23-24 (canceled)

25. (currently amended) The integrated circuit chip according to claim 15, wherein said nitride ~~passivation layer~~ comprises silicon nitride.

Claim 26 (canceled)

27. (currently amended) The integrated circuit chip according to claim 15, wherein said third contact pad comprises a gold layer.

Claim 28 (canceled)

29. (withdrawn – currently amended) The integrated circuit chip according to claim 15 further comprising a second polymer layer ~~over~~ on said passivation layer, wherein said second contact pad and said first polymer layer are further ~~is~~ on said second polymer layer.

30. (withdrawn) The integrated circuit chip according to claim 29, wherein said second polymer layer comprises polyimide.

Claims 31-90 (canceled)

91. (currently amended) The integrated circuit chip according to claim 1, wherein said nitride ~~passivation layer~~ comprises silicon nitride.

Claims 92-95 (canceled)

96. (previously presented) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a nickel layer over said copper layer of said ground metal structure.

97. (currently amended) The integrated circuit chip according to claim 1 further comprising a polymer layer ~~over~~ on said power and ground metal structures, wherein a third opening in said polymer layer is over a third contact point of said power metal structure, and said third contact point is at a bottom of said third opening, ~~exposes said power metal structure,~~ and wherein a fourth opening in said polymer layer is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening, ~~exposes said ground metal structure, and~~ wherein said first solder contact ~~connection~~ is between said capacitor and said third contact point and connects said

capacitor to said third contact point ~~power metal structure~~ through said third opening, and said second solder contact ~~connection~~ is between said capacitor and said fourth contact point and connects said capacitor to said fourth contact point ~~ground metal structure~~ through said fourth opening.

98. (previously presented) The integrated circuit chip according to claim 9, wherein said capacitor comprises a decoupling capacitor.

99. (previously presented) The integrated circuit chip according to claim 9, wherein said nitride comprises silicon nitride.

Claim 100 (canceled)

101. (previously presented) The integrated circuit chip according to claim 15, wherein said capacitor comprises a decoupling capacitor.

102. (currently amended) The integrated circuit chip according to claim 15, wherein a third opening in said first polymer layer is over said region of said third contact pad, and ~~exposes~~ said region ~~third contact~~ is at a bottom of said third opening. ~~pad.~~

103. (previously presented) The integrated circuit chip according to claim 15, wherein said

first polymer layer comprises polyimide.

Claims 104-107 (canceled)

108. (new) The integrated circuit chip according to claim 15, wherein said first polymer layer has a thickness between 2 and 150 micrometers.

109. (new) The integrated circuit chip according to claim 15, wherein a ground voltage is applied to said first, second and third contact pads.

110. (new) The integrated circuit chip according to claim 15, wherein a power supply voltage is applied to said first, second and third contact pads.

111. (new) The integrated circuit chip according to claim 15, wherein said passivation layer further comprises an oxide.

112. (new) The integrated circuit chip according to claim 15, wherein said passivation layer further comprises silicon oxide.

113. (new) The integrated circuit chip according to claim 97, wherein said polymer layer comprises polyimide.

114. (new) The integrated circuit chip according to claim 97, wherein said polymer layer has a thickness between 2 and 150 micrometers.

115. (withdrawn - new) The integrated circuit chip according to claim 4, wherein said polymer layer comprises polyimide.

116. (new) The integrated circuit chip according to claim 1, wherein said passivation layer further comprises an oxide.

117. (new) The integrated circuit chip according to claim 1, wherein said passivation layer further comprises silicon oxide.

118. (new) The integrated circuit chip according to claim 12, wherein said fourth contact pad comprises a second gold layer.

119. (new) The integrated circuit chip according to claim 9 further comprising a polymer layer over said passivation layer, wherein a second opening in said polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening, and wherein said solder contact is between said capacitor and said second contact point and connects said capacitor to said second contact point through said second opening.

120. (new) The integrated circuit chip according to claim 119, wherein said polymer layer has a thickness between 2 and 150 micrometers.

121. (new) The integrated circuit chip according to claim 9, wherein said passivation layer further comprises an oxide.

122. (new) The integrated circuit chip according to claim 9, wherein said passivation layer further comprises silicon oxide.

123. (new) The integrated circuit chip according to claim 1 further comprising a polymer layer on said power and ground metal structures, wherein a third opening in said polymer layer is over said first region, and said first region is at a bottom of said third opening, and wherein a fourth opening in said polymer layer is over said second region, and said second region is at a bottom of said fourth opening.

124. (new) The integrated circuit chip according to claim 123, wherein said polymer layer comprises polyimide.

125. (new) The integrated circuit chip according to claim 123, wherein said polymer layer has a thickness between 2 and 150 micrometers.

126. (new) The integrated circuit chip according to claim 1 further comprising a polymer layer on said power and ground metal structures, wherein a third opening in said polymer layer is over a third contact point of said power metal structure, and said third contact point is at a bottom of said third opening, wherein a fourth opening in said polymer layer is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening, wherein a fifth opening in said polymer layer is over said first region, and said first region is at a bottom of said fifth opening, and wherein a sixth opening in said polymer layer is over said second region, and said second region is at a bottom of said sixth opening, wherein said first solder contact is between said capacitor and said third contact point and connects said capacitor to said third contact point through said third opening, and said second solder contact is between said capacitor and said fourth contact point and connects said capacitor to said fourth contact point through said fourth opening.

127. (new) The integrated circuit chip according to claim 126, wherein said polymer layer comprises polyimide.

128. (new) The integrated circuit chip according to claim 126, wherein said polymer layer has a thickness between 2 and 150 micrometers.

129. (new) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein said passivation layer comprises a nitride;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact point, and wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and over said second contact pad;

a solder contact between said capacitor and said second contact pad, wherein said solder contact connects said capacitor to said second contact pad; and

a third contact pad between said solder contact and said second contact pad, wherein said third contact pad is finished with a solder wettable material comprising gold.

130. (new) The integrated circuit chip according to claim 129 further comprising a fourth contact pad over said semiconductor substrate, wherein said fourth contact pad has a second contact point under a second opening in said passivation layer, and said second contact point is at a bottom of said second opening, wherein said second contact point is used to be wirebonded thereto for connection made to a next level of packaging.

131. (new) The integrated circuit chip according to claim 129 further comprising a fourth contact pad over said passivation layer, wherein said fourth contact pad is used to be wirebonded thereto for connection made to a next level of packaging.

132. (new) The integrated circuit chip according to claim 129 further comprising a fourth contact pad over said semiconductor substrate, wherein said fourth contact pad has a second contact point under a second opening in said passivation layer, and said second contact point is at a bottom of said second opening, and a fifth contact pad on said second contact point, wherein said fifth contact pad is used to be wirebonded thereto for connection made to a next level of packaging.

133. (new) The integrated circuit chip according to claim 132, wherein said fifth contact pad comprises a second gold layer.

134. (new) The integrated circuit chip according to claim 129, wherein said capacitor comprises a decoupling capacitor.

135. (new) The integrated circuit chip according to claim 129, wherein said nitride comprises silicon nitride.

136. (new) The integrated circuit chip according to claim 129 further comprising a polymer layer over said passivation layer, wherein a second opening in said polymer layer is over a

second contact point of said second contact pad, and said second contact point is at a bottom of said second opening, and wherein said solder contact is between said capacitor and said second contact point and connects said capacitor to said second contact point through said second opening.

137. (new) The integrated circuit chip according to claim 136, wherein said polymer layer has a thickness between 2 and 150 micrometers.

138. (new) The integrated circuit chip according to claim 129, wherein said passivation layer further comprises an oxide.

139. (new) The integrated circuit chip according to claim 129, wherein said passivation layer further comprises silicon oxide.